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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,918	11/14/2003	Mitsuyoshi Mori	60188-710	7667

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/706,918	MORI ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments to the claims filed 24 October 2006 have been entered. The rejections under 35 USC §112 of claims 37 and 38 have been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **34-47, 49-63, 65 and 68** are rejected under 35 U.S.C. 102(b) as being anticipated by Guidash (US 6,352,869).

4. Regarding claims **34-35, 39-42, 44, 49, 51 and 62**, the '869 patent discloses in Figures 2A and 2B a solid state imaging apparatus comprising: a plurality of photoelectric conversion cells (one shown) each including a plurality of photoelectric sections of photodiodes arranged in a matrix including at least first and second rows and first and second columns (one column shown); a plurality of first floating diffusion sections (FD, item 26, one shown shared between adjacent row pixels) provided between said photoelectric conversion cells (see Fig 2A, FD is between cells in the column diretion), each being shared by, and being connected to, the photoelectric sections (photodiodes PD1, PD2) which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors (TG1, TG2), respectively; a plurality of second floating diffusion sections (in the next column not

shown) each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively; a plurality of read-out lines (col 2 ln 24-28) each being selectively connected to the transfer transistors (TG1 and other transistors on pixels in the same row, or TG2 and other transistors on pixels in the same row) connected to the photoelectric conversion sections which are included in one of the first and second columns; a plurality of first pixel amplifier transistors (27) coupled to and detecting and outputting the potential of each first floating diffusion section; a plurality of second pixel amplifier transistors (in the next row not shown) coupled to and detecting and outputting the potential of each second floating diffusion section, wherein the first and second pixel amplifiers comprises a source follower transistor (col 2 ln 26).

5. Regarding claim **36**, the '869 patent discloses the apparatus of claim 39, wherein the plurality of read lines are connected to a vertical scanning circuit (col 2 ln 19, each row is read at a time, therefore the array is scanned vertically).

6. Regarding claims **37-38 and 43**, the '869 patent discloses the apparatus of claim 39, wherein a plurality of a pair of signal lines (one shown, column output buss) outputs signals from the first pixel amplifier (27) and the second pixel amplifier (not shown, in an adjacent column) to the outside, wherein a select transistor (29) is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier and the signal line.

7. Regarding claims **45 and 50**, the '869 patent discloses the apparatus of claims 39 and 49, further comprising a reset transistor (28), wherein the drain of the reset

transistor is connected to the drain of the pixel amplifier transistor (Fig 2A, both connect to node VDD) so that a drain is shared by the reset transistor and the pixel amplifier transistor.

8. Regarding claims **46 and 63**, the '869 patent discloses the apparatus of claims 39 and 49, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction (see distance between PD sections in Fig 2A).

9. Regarding claims **47 and 65**, the '869 patent discloses in Fig 2B the apparatus of claims 39 and 49, further comprising a signal processing circuit (bottom dotted outline box) for processing an output signal from each pixel amplifier transistor (27).

10. Regarding claims **53-55 and 57-60**, the '869 patent discloses in Fig 2A the apparatus of claims 49 and 50, wherein each pixel amplifier transistor (27) and each reset transistor (28) is arranged between rows (two rows shown with one pixel each: PDa and PDb) and between the photoelectric cells which are adjacent to each other in the row and column direction (amplifier transistors are to the right side of each column, reset transistors are to the left of each column and between rows), which include some of the photoelectric conversion section and are adjacent to each other in each said photoelectric conversion cell. Each amplifier transistor and each floating diffusion section are arranged between the read out lines (items 29, one per row).

11. Regarding claims **52, 56 and 61**, the '869 patent discloses in Fig 2A the apparatus of claims 49, 55 and 60, wherein each said transfer transistor (TG1, TG2) is made of an MIS transistor (metal on insulator as shown in Fig 2B) and wherein a gate of

the MIS transistor is arranged in the row direction, and wherein each pixel amplifier transistor (27) and each reset transistor (28) is arranged between respective gates of the MIS transistor and another MIS transistor (e.g., a transistor in another column or between the two transfer gates in the figure's vertical direction).

12. Regarding claim **68**, the '869 patent discloses in Fig 2B the apparatus of claim 39, wherein respective charges of the photoelectric conversion sections (PD1) each connected to one of the read-out lines and being read out by the transfer transistors (TG1) are read out by said first floating diffusion section (FD).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims **66, 67 and 69** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent and Patterson (US 6,541,794).

16. Regarding claims **66 and 67,** the '869 patent discloses each limitation as claimed in claim 39 except for disclosing that the solid state imaging apparatus is part of a camera. Patterson teaches that arrays of photoactive pixel circuits are used in cameras (col 1 ln 11) since they are suitable for capturing images projected onto the arrays (col 1 ln 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Patterson on the array disclosed by the '869 patent in order to capture images.

17. Regarding claim **69**, the '869 patent discloses in Fig 2B the apparatus of claim 39, wherein respective charges of the photoelectric conversion sections (PD1) each connected to one of the read-out lines and being read out by the transfer transistors (TG1) are read out by said first floating diffusion section (FD).

18. Claims **48 and 64** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent as applied to claim 39 above and further in view of Yamazaki (US 2002/0145582).

The '869 patent discloses each limitation as claimed in claims 39 and 50, but does not specify that the sections are separated from one another by a power supply line which also functions as a light-shielding film, or that the shared line (V_{DD}) of the reset transistor and output transistor functions as a light-shielding film.

Yamazaki teaches the use of a power supply line between pixels (or sections), which is also used as a light shield in order to protect the channel formation regions and p type semiconductor regions (¶ 90). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Yamazaki on the structure of the '869 patent in order to use the power supply line as a light shield for channel and p type regions between pixels and/or pixel sections. Since V_{DD} is a power supply line, it follows that the shared line of the reset transistor and output transistor would also be used as a light shield.

Response to Arguments

19. Applicant's arguments filed 24 October 2006 have been fully considered but they are not persuasive. Regarding the argument on page 14 that the FD section of the '869 patent are not connected to different amplifiers, Fig 2 shows an arrangement with two adjacent pixels (in the same column) sharing an amplifier in a row direction, meaning that two adjacent columns will have two amplifiers. The FD section and amplifier is provided between the pixels in the same column.

20. Applicant's arguments with respect to Hashimoto, Yamazaki, Patterson, and '323 patent have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham
Examiner
Art Unit 2814

jci